**LISTING OF THE CLAIMS:**

Claims 1-41 (Previously Cancelled)

Claim 42 (Withdrawn) A layered structure for forming electrical devices thereon comprising:

a single crystalline substrate,

a first layer of relaxed $Si_{1-x}Ge_x$ formed epitaxially on said substrate where Ge fraction x is in the range from 0.35 to 0.5,

an over-shoot layer, $Si_{1-y}Ge_y$, within the relaxed structure of said first layer having a Ge fraction y, where $y = x + z$ and z is in the range from 0.01 to 0.1, and having a thickness less than its critical thickness with respect to the top of said first layer, and

a second layer of $Si_{1-x}Ge_x$ formed epitaxially on said first layer.

Claim 43 (Currently Amended) A method for forming p-channel field effect transistors comprising the steps of:

selecting a single crystalline substrate,

forming a first layer of relaxed $Si_{1-x}Ge_x$ ~~formed~~ epitaxially on said substrate where Ge fraction x is in the range from 0.35 to 0.5,

forming a second layer of $Si_{1-x}Ge_x$ epitaxially on said first layer,

forming a third layer of undoped Si [[f]] epitaxially on said second layer,

forming a fourth layer of undoped $Si_{1-x}Ge_x$ [[f ]]epitaxially on said third layer,

forming a fifth layer of Ge epitaxially on said fourth layer whereby said fifth layer is

under compressive strain and has a thickness less than its critical thickness with respect to said first layer,

forming a sixth layer of $Si_{1-w}Ge_w$ epitaxially on said fifth layer where the Ge fraction w is in the range from 0.5 to <1.0 and where w-x > 0.2 whereby said sixth layer is under compressive strain, and

forming a seventh layer of $Si_{1-x}Ge_x$ epitaxially on said sixth layer.

Claim 44 (Currently Amended) The method of claim 43 further including the steps of forming an over-shoot layer, $Si_{1-y}Ge_y$, within ~~the~~ a strain relief structure of said first layer having a Ge fraction y, where $y = x \pm z$ and z is in the range from 0.01 to 0.1, and having a thickness less than its critical thickness with respect to said first layer.

Claim 45 (Original) The method of claim 43 wherein said fifth layer is formed at temperatures where 3D growth of Ge films does not occur to generate interface roughness problems and at a temperature range from 275° - 350° C where 2D growth of Ge films does occur.

Claim 46 (Currently Amended) The method of claim 43 wherein said step of forming a said sixth layer includes the step of grading the Ge content w within said sixth layer starting with a higher Ge content nearer said fifth layer and grading down in Ge content towards the upper surface of said sixth layer.

Claim 47 (Amended) The ~~layered structure~~ method of claim 43 wherein said

second layer is a p-doped $Si_{1-x}Ge_x$ layer formed below a channel region of said fifth and sixth layers and separated therefrom by said third layer of Si and said fourth layer of $Si_{1-x}Ge_x$, said second layer ~~is to~~ having a thickness in the range from 1 to 20 nm with a preferred thickness from 4 to 5 nm and having an electrically active donor dose in the range from 1 to $3x10^{12}$ $cm^{-2}$.

Claim 48 (Currently Amended) A method for forming p-channel field effect transistors comprising:

selecting a single crystalline substrate,

forming a first layer of relaxed $Si_{1-x}Ge_x$ epitaxially on said substrate where Ge fraction x is in the range from 0.35 to 0.5,

forming a second layer of $Si_{1-x}Ge_x$ [[f]] epitaxially on said first layer,

forming a third layer of undoped Si [[f]] epitaxially on said second layer,

forming a fourth layer of Ge epitaxially on said third layer whereby said fourth layer is under compressive strain and having a thickness less than its critical thickness with respect to said first layer,

forming a fifth layer of [[$Si_{1w}Ge_w$]] $\underline{Si_{1-w}Ge_w}$ epitaxially on said fourth layer wherein the Ge fraction w is in the range from 0.5 to <1.0 and where w-x > 0.2 whereby said fifth layer is under compressive strain, and

forming a sixth layer of $Si_{1-x}Ge_x$ epitaxially on said fifth layer.

Claim 49 (Currently Amended) The method of claim 48 further including the step of forming an over-shoot layer, $Si_{1-y}Ge_y$ within ~~the~~ a strain relief structure of said first

layer having a Ge fraction y, where $y = x + z$ and $z$ is in the range from 0.01 to 0.1, and having a thickness less than its critical thickness with respect to said first layer.

Claim 50 (Currently Amended) The ~~layered structure~~ method of claim 48 wherein said fourth layer is formed at temperatures where 3D growth of Ge films does not occur to generate interface roughness problems and at a temperature range from 275° - 350°C where 2D growth of Ge films does occur.

Claim 51 (Currently Amended) The ~~layered structure~~ method of claim 48 wherein said step of forming ~~a sixth~~ the fifth layer includes the step of grading the Ge content w ~~may be graded~~ within said fifth layer starting with a higher Ge content nearer said fourth layer and grading down in Ge content towards the upper surface of said fifth layer.

Claim 52 (Currently Amended) The method of claim 48 wherein said third layer of undoped Si may be substituted with a relaxed $Si_{1-x}Ge_x$ layer with an adjustable thickness to allow ~~the~~ for a spacer thickness to be varied accordingly whereby ~~the~~ a supply dose may be optimized for device applications as a function of temperature in the range from 0.4 to 425K.[[.]]

Claim 53 (Currently Amended) The method of claim 48 wherein said second layer of ~~p-doped~~ $Si_{1-x}Ge_x$ layer is formed below a channel region of said fourth and fifth layers and separated therefrom by said third layer of Si.

Claim 54 (Currently Amended) The method of claim 52 wherein ~~the~~ a supply layer of said second layer is formed and separated below ~~the~~ a channel region of said fourth and fifth layers by said relaxed layer $Si_{1-x}Ge_x$.

Claim 55 (Currently Amended) A method for forming p-channel field effect transistors comprising:

selecting a single crystalline substrate,

forming a first layer of relaxed $Si_{1-x}Ge_x$ epitaxially on said substrate where Ge fraction x is the range from 0.35 to 0.5,

forming a second layer of Ge epitaxially on said first layer whereby said second layer is under compressive strain and having a thickness less than its critical thickness with respect to said first layer,

forming a third layer of $Si_{1-w}Ge_w$ [[f]] epitaxially on said second layer where the Ge fraction w is in the range from 0.5 to <1.0 and where w-x>0.2 whereby said third layer is under compressive strain,

forming a fourth layer of undoped $Si_{1-x}Ge_x$ epitaxially on said third layer,

forming a fifth layer of undoped Si epitaxially on said fourth layer, and

forming a sixth layer of p-doped $Si_{1-x}Ge_x$ epitaxially on said fifth layer.

Claim 56 (Currently Amended) The method of claim 55 further including an over-shoot layer, $Si_{1-y}Ge_y$, within ~~the~~ a strain relief structure of said first layer having a Ge fraction y, where $y = x + z$ and $z$ is in the range from 0.01 to 0.1, and having a thickness less than its critical thickness with respect to said first layer.

Claim 22 (Previously Cancelled)

Claim 57 (Original) The method of claim 55 wherein said second layer is formed at temperatures where 3D growth of Ge films does not occur to generate interface roughness problems and at a temperature range from 275° - 350°C where 2D growth of Ge films does occur.

Claim 58 (Currently Amended) The ~~layered structure~~ method of claim 55 wherein said step of forming ~~a~~ the third layer includes the step of grading the Ge content w within said third layer starting with a higher content nearer said second layer and grading down in Ge content towards the upper surface of said third layer.

Claim 59 (Currently Amended) The method of claim 55 wherein ~~the~~ a supply layer of p-doped $Si_{1-x}Ge_x$ layer of said sixth layer is formed above a channel region of said second and third layers and is separated by a composite spacer structure of said fifth layer of Si and said fourth layer of $Si_{1-x}Ge_x$.

Claim 60 (Currently Amended) A method for forming p-channel field effect transistors comprising:

selecting a single crystalline substrate,

forming a first layer of relaxed $Si_{1-x}Ge_x$ epitaxially on said substrate where Ge fraction x is the range from 0.35 to 0.5,

forming a second layer of Ge epitaxially on said first layer whereby said second

layer is under compressive strain and has a thickness less than its critical thickness with respect to said first layer,

forming a third layer of $Si_{1-w}Ge_w$ [[f]] epitaxially on said second layer where the Ge fraction w is in the range from 0.5 to <1.0 and where w-x> 0.2 whereby said third layer is under compressive strain,

forming a fourth layer of undoped $Si_{1-x}Ge_x$ epitaxially on said third layer, and

a fifth layer of p-doped $Si_{1-x}Ge_x$ formed epitaxially on said fourth layer.

Claim 61 (Currently Amended) The method of claim 60 further including the step of forming an over-shoot layer, $Si_{1-y}Ge_y$, within ~~the~~ a strain relief structure of said first layer having a Ge fraction y, where $y = x \pm z$ and $z$ is in the range from 0.01 to 0.1, and having a thickness less than its critical thickness with respect to said first layer.

Claim 62 (Original) The method of claim 60 wherein said second layer is formed at temperatures where 3D growth of Ge films does not occur to generate interface roughness problems and at a temperature range from 275° - 350°C where 2D growth of Ge films does occur.

Claim 63 (Currently Amended) The method of claim 60 wherein said step of forming ~~a~~ the third layer includes the step of grading the Ge content w within said third layer starting with a higher content nearer said second layer and grading down in Ge content towards the upper surface of said third layer.

Claim 64 (Original) The method of claim 60 wherein said fifth layer is a p-doped $Si_{1-x}Ge_x$ layer formed above a channel region of said second and third layers and separated therefrom by said fourth layer of $Si_{1-x}Ge_x$.

Claim 65 (Original) The ~~layered structure~~ method of claim 60 wherein said fifth layer is a p-doped $Si_{1-x}Ge_x$ layer formed above a channel region of said second and third layers and separated therefrom by a thin strained commensurate Si layer.

Claim 66 (Original)A method of forming a field-effect transistor structure consisting of the method of claim 43, further comprising the steps of,

forming electrical isolation regions by the selective removal of at least said seventh through second layer,

forming a Schottky gate electrode on said seventh layer,

forming a source electrode located on one side of said gate electrode, and

forming a drain electrode located on the other side of said gate electrode.

Claim 67 (Original) A method for forming a field-effect transistor structure consisting of the method of claim 48, further comprising the steps of,

forming electrical isolation regions by the selective removal of at least said sixth through second layer,

forming a Schottky gate electrode on said sixth layer,

forming a source electrode located on one side of said gate electrode, and

forming a drain electrode located on the other side of said gate electrode.

Claim 68 (Currently) A method of forming a field-effect transistor structure consisting of the method of claim ~~1~~ 55, further comprising,

forming electrical isolation regions by the selective removal of at least said seventh through second layer,

forming a gate dielectric on said seventh layer, forming a gate electrode on said gate dielectric,

forming a source electrode located on one side of said gate electrode, and

forming drain electrode located on the other side of said gate electrode.

Claim 69 (Currently Amended) A method of forming a field-effect transistor structure consisting of the method of claim 48, further comprising the steps of,

forming electrical isolation regions by the selective removal of at least said sixth through second layer,

forming a gate dielectric [[f]] on said sixth layer,

forming a gate electrode on said gate dielectric,

forming a source electrode located on one side of said gate electrode, and

forming drain electrode located on the other side of said gate electrode.

Claim 70 (Original) A method for forming a field-effect transistor structure consisting of the method of claim 55, further comprising,

forming electrical isolation regions by the selective removal of at least said sixth through second layer,

forming a gate dielectric on said sixth layer,

forming a gate electrode on said gate dielectric,

forming a source electrode located on one side of said gate electrode, and

forming a drain electrode located on the other side of said gate electrode.

Claim 71 (Original) A method of forming a field-effect transistor structure consisting of the method of claim 60, further comprising,

forming electrical isolation regions by the selective removal of at least said fifth through second layer,

forming a gate dielectric formed on said fifth layer,

forming a gate electrode on said gate dielectric,

forming a source electrode located on one side of said gate electrode, and

forming a drain electrode located on the other side of said gate electrode.

Claim 72 (Currently Amended) A method for forming electrical devices comprising the steps of:

forming a single crystalline substrate,

forming a first layer of relaxed $Si_{1-x}Ge_x$ formed epitaxially on said substrate where Ge fraction x is in the range from 0.35 to 0.5,

forming an over-shoot layer, $Si_{1-y}Ge_y$, within ~~the~~ a relaxed structure of said first layer having a Ge fraction y, where $y = x + z$ and $z$ is in the range from 0.01 to 0.1, and having a thickness less than its critical thickness with respect to the top of said first layer, and

forming a second layer of $Si_{1-x}Ge_x$ formed epitaxially on said first layer.